Options for Blockchain Acceleration on SmartNICs

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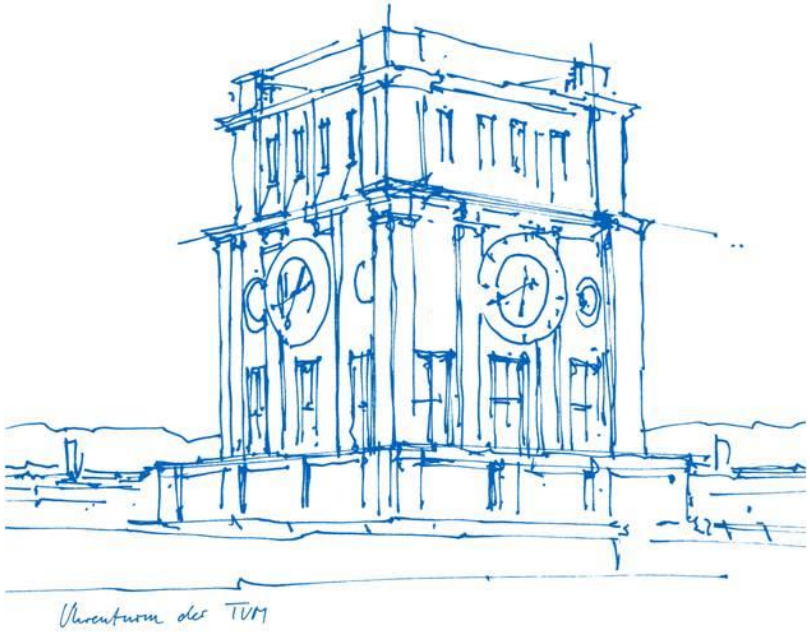


Outline

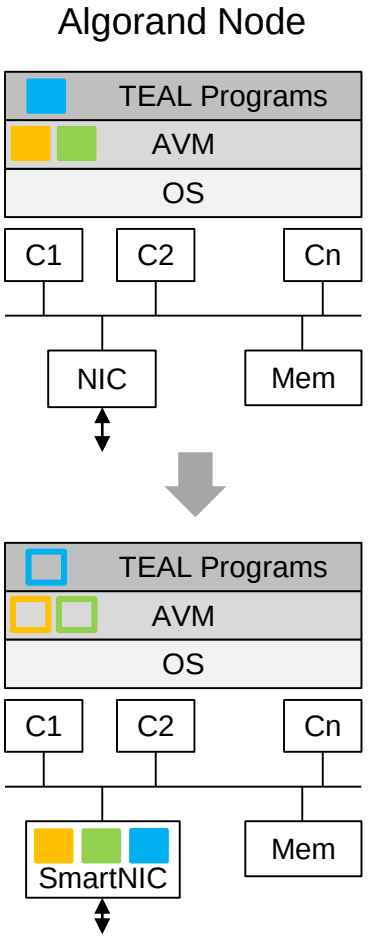
1. Overview
2. Acceleration Options
3. Hardware / Software Codesign
4. SmartNIC Platforms
5. Summary

Overview

Targets

- Investigate potential of SmartNIC-based hardware acceleration (offload host CPUs)
  - to increase performance in terms of
    - higher throughput and/or
    - lower latencies,
  - to reduce power dissipation

- Apply acceleration for
  - Algorand-specific functions
    (message relaying and forwarding;
    sub-tasks of validation functions),
  - Generic networking functions
    (packet header parsing, packet modification).



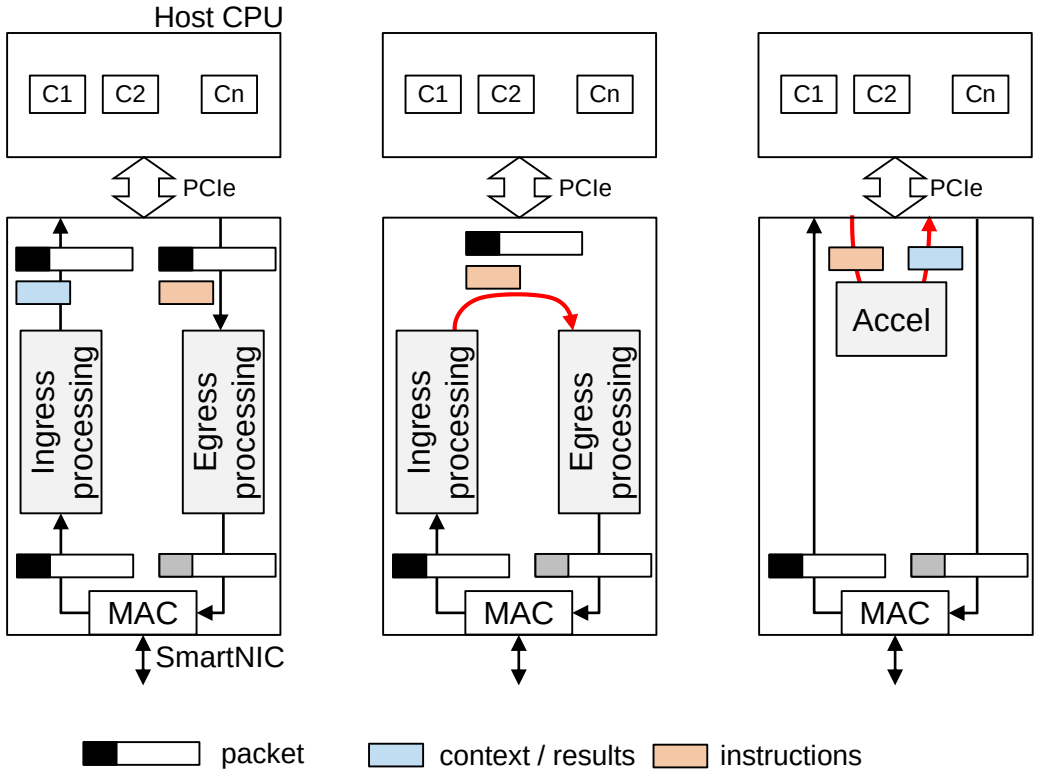
Generic Options for SmartNIC-based Acceleration

Reconfigurable hardware data path with deterministic latency on the FPGA
Resources of a SmartNIC

- Ingress pre-processing, egress post-processing
- Hardware only data path (w/o host involvement)

Acceleration of specific sub-functions as part of software processing chain

- Call from a host CPU

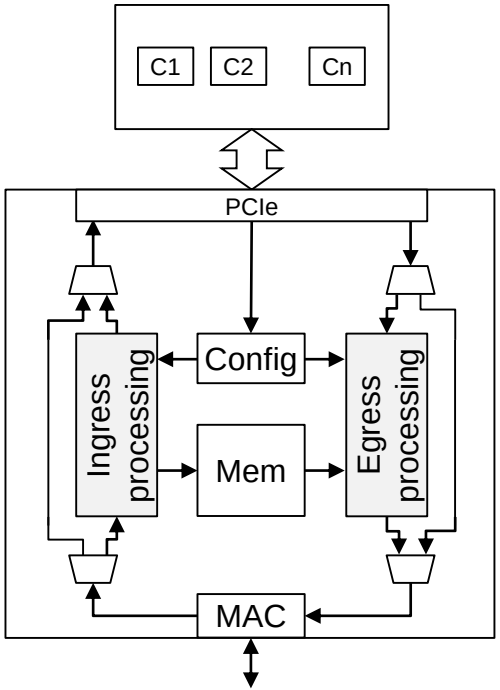


SmartNIC-based Acceleration - HW/SW Codesign

Frames can bypass ingress/egress processing

- Full software-based processing on **host CPU** for
  - standard/non-blockchain functions
  - complex functions
  - functions to control SmartNIC-based acceleration

- **SmartNIC**-based ingress/egress processing
  - controlled by software running on host CPU
  - processing on frame or message level
  - local storage of frames/messages and context information



SmartNIC-based Acceleration for Algorand

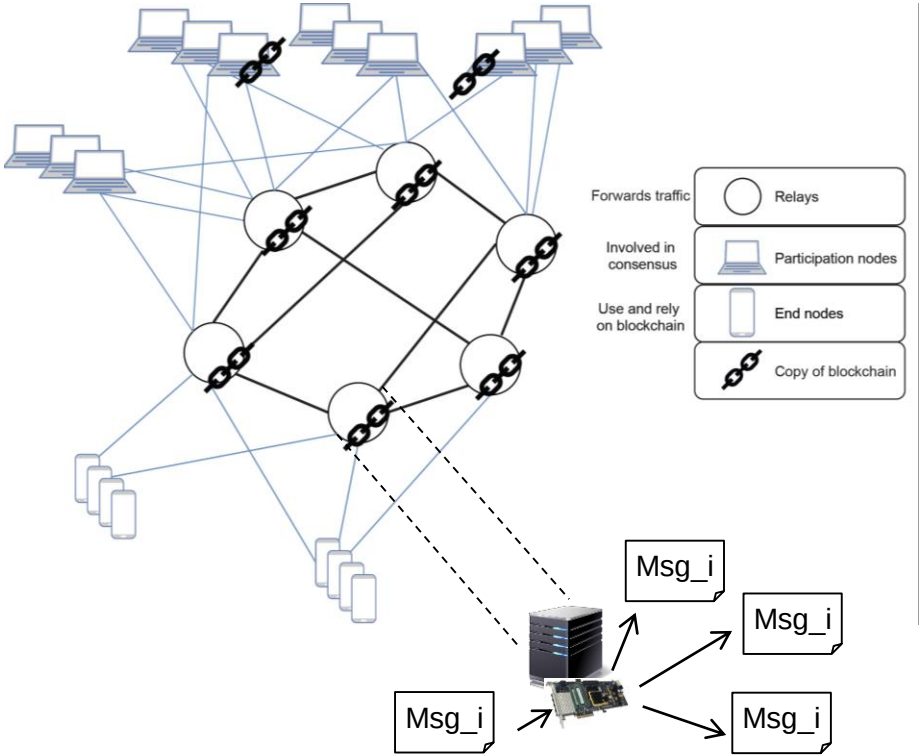
Relay nodes as candidates for SmartNIC

Potential functionalities in the consensus process to be accelerated

- message relaying / forwarding
- associated compute-intensive functions

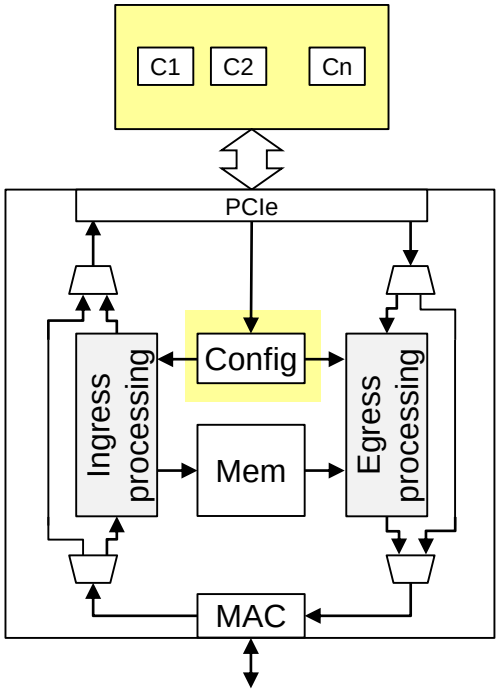
- Message types to be relayed (size up to 5 MiB):
  - Transactions
  - Blocks
  - Consensus messages

All packets making up a message to be sent to a set of relay or participating nodes.



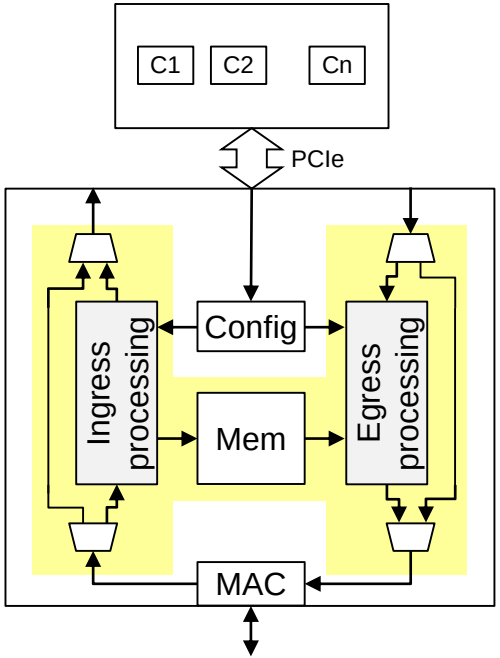
SmartNIC-based Acceleration for Algorand

- Setup membership in Algorand Network
- Establish connections to peer relay nodes
- Provide transport protocol port number to listen for Algorand packets
- Provide keys for message authentication
- Provide target addresses for relay targets

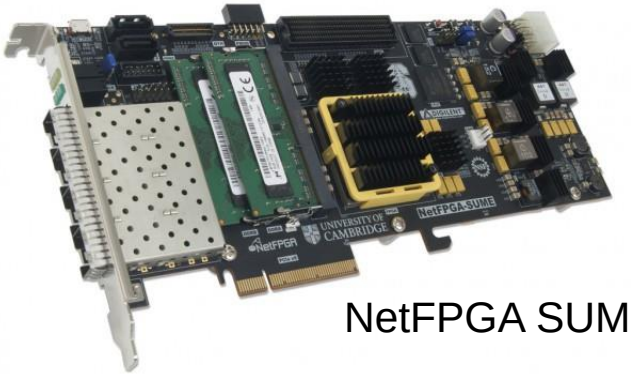


SmartNIC-based Acceleration for Algorand

- Packet parsing/classification: identify individual messages and their types and all associated packets
- Store Algorand messages to be relayed
- Verification / authentication of messages
- Prevent multiple relaying of messages based on hash
- Send copies of message / packets to recipients



FPGA Based SmartNIC Platforms



NetFPGA SUME

- 4x 10G Ethernet
- Xilinx Virtex-7 XC7V690T
- PCIe Gen3 x8
  (no DPDK support)

Alveo U55C

- 2x 100G Ethernet
  (with breakout cable also usable as 4x25G or 4x10G)
- UltraScale+ XCU55C FPGA
- PCIe Gen3 x16, PCIe Gen4 x8
  (PCIe IP core with DPDK support)

Summary

- SmartNICs as potential blockchain accelerator
- First target function: message relaying for Algorand
- In-depth analysis of relaying function in GO software implementation
- Next steps:
  - Detailed specification of hardware/software interfaces
  - Stepwise implementation of associated sub-functions
  - Extend available hardware processing data path
  - Porting to FPGA based SmartNiC